In the claims:

1-24 (canceled)

1. ~~25.~~ (currently amended) A method of fabricating an SOI structure which comprises the steps of:

D1

(a) providing a substrate having at least one of active or passive elements on a surface thereof;

(b) providing [and] a device wafer having at least one of active or passive elements on a surface thereof;

(c) forming an electrically insulating layer having a pair of opposed outer faces, one of said opposed outer faces disposed on a said surface of one of said substrate or said device wafer, said electrically insulating layer having an electrical interconnect structure disposed therewithin, a portion of said interconnect structure extending substantially to said one of said outer faces of said electrically insulating structure to make electrical contact with a device in at least one of the device wafer and the substrate; and

(d) then bonding the other of said outer faces of said electrically insulating layer to the said surface of the other of said substrate or device wafer;

~~The method of claim 1~~ further including the steps of forming an electrical insulation on at least one of said electrically insulating layer, said substrate or said device wafer insulating said interconnect structure from said device in said at least one of the device wafer and the substrate and applying a voltage across said electrical insulation to break down said electrical insulation an provide interconnection between said interconnect structure and said device.

D

2. ~~26.~~ (currently amended) A method of forming an SOI structure, comprising the steps of:

providing a device layer having at least one of active or passive elements on a surface thereof;

providing a substrate having at least one of active or passive elements on a surface thereof; [and]

providing an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof;

D1 Cont.

forming a substantially planar region on said surface of said device layer and said surface of said substrate;

forming a substantially planar region on said surface of said electrically insulating layer;

interposing said electrically insulating layer between said device layer and said substrate with said planar region of said electrically insulating layer overlaying said substantially planar region on said at least one of said surface of said device layer and said surface of said substrate to make electrical contact with a device in at least one of the device wafer and the substrate; and

then bonding said planar surface of said electrically insulating layer to [the other of] said overlying one of said substrate and said device layer.

~~The method of claim 7~~ further including the steps of forming an electrical insulation on at least one of said electrically insulating layer, said substrate or said device wafer insulating said interconnect structure from said device in said at least one of the device wafer and the substrate and applying a voltage across said electrical insulation to break down said electrical insulation an provide interconnection between said interconnect structure and said device.